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10/827,433	04/20/2004	Fumitoshi Mizutani	089367-0127	2720

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EXAMINER	
REDDIVALAM, SRINIVASA R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/827,433	MIZUTANI ET AL.	
	Examiner	Art Unit	
	SRINIVASA R. REDDIVALAM	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on March 11th, 2008 has been entered. Claims 1 and 12-16 have been amended. Claims 1-16 are still pending in this application, with claims 1, 6, 7, and 12 being independent.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 7, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Horvath et al. (US Patent Number: 5,630,056)

Regarding claim 1, Horvath et al. teach a data processing apparatus that has a plurality of reception interface sections which receive same data from a same data sender and processes data (see col.2, lines 25-32 wherein a digital data processing device with plurality of functional units processing data in parallel is mentioned and col.2, lines 54-59 wherein transceivers, which include both transmitters and receivers, routing data is mentioned), received by said plurality of reception interface sections, in parallel, wherein each of said reception interface sections includes a communication error processing section which (see col.2, lines 54-59 wherein transceivers routing data

to the fault-detector is mentioned), upon occurrence of an error in said received data, stops receiving said data, sends a communication error signal to other reception interface sections to stop data reception from said data sender, and requests said data sender to resend data (see col.2, lines 32-36 wherein fault-detector signaling a fault is mentioned and col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals and responding to the error by reapplying the data is mentioned. And also Fig.1 and col.3, line 55 to col.4, line 2 wherein functional units i.e. processor/memory elements 10, 12 **partnered with one another to respond concurrently and identically** to information input from bus 20 to generate further information for output to bus 20 is mentioned, likewise peripheral device controllers 14, 16 partnered with one another to process and communicate like information between the functional units and peripheral devices is mentioned).

Regarding claims 2 and 3, Horvath et al. further teach the data processing apparatus, wherein when an error occurs in part of received data, said communication error processing section of each of said reception interface sections cancels said error-occurred data, and requests said data sender to resend said canceled data (see col.2, lines 37-53 wherein upon detection of an error by fault-detector, disabling of data processing by functional unit and re-transmission of respective data by processing sections are mentioned) and wherein said data sender sends same serial data (see col.2, lines 54-59 wherein transceiver routing data is mentioned), and when an error occurs in received serial data, said communication error processing section of each of said reception interface sections cancels said error-occurred serial data and serial data

received following that error-occurred serial data, and requests said data sender to resend said canceled serial data (see col.2, lines 47-53 and lines 58-65 wherein upon detection of an error by fault-detector, disabling of processing section from applying data and re-transmission of serial data by transceiver to fault-detector are mentioned).

Regarding claim 7, Horvath et al. teach a data processing method that performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender (see col.2, lines 25-32 wherein a digital data processing device with plurality of functional units processing data in parallel is mentioned and col.2, lines 54-59 wherein transceivers routing data is mentioned) and comprises: a data reception step of receiving data from said data sender at one of said plurality of reception interface sections (see col.2, lines 54-59 wherein transceivers sending data to fault-detector is mentioned); an error detection step of detecting an error in said received data (see col.2, lines 32-36 wherein fault-detector signaling a fault of received data is mentioned); and an error information output step of outputting information on said detected error to other reception interface sections (see col.2, lines 37-46 and lines 59-65 wherein response of transmission error among transceivers is mentioned).

Regarding claim 12, Horvath et al. teach a computer readable medium having thereon a computer program, which when executed, (see col.4, lines 60-62 wherein a device implementation in software/hardware is mentioned) performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender (see col.2, lines 25-32 wherein a digital data processing

device with plurality of functional units processing data in parallel is mentioned and col.2, lines 54-59 wherein transceivers routing data is mentioned) and allows a computer to execute: a data reception step of receiving data from said data sender at one of said plurality of reception interface sections (see col.2, lines 54-59 wherein transceivers sending data to fault-detector is mentioned); an error detection step of detecting an error in said received data (see col.2, lines 32-36 wherein fault-detector signaling a fault of received data is mentioned); and an error information output step of outputting information on said detected error to other reception interface sections (see col.2, lines 37-46 and lines 59-65 wherein response of transmission error among transceivers is mentioned).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horvath et al. (US Patent Number: 5,630,056) in view of Horst et al. (US Patent No: 6,496,940).

Regarding claim 4, Horvath et al. teach the data processing apparatus wherein data sender sends data packet when an error occurs in data of the received packet (see col.2, lines 62-65) and said communication error processing section of each of said reception interface sections requests said data sender to resend data (see col.2, lines 32-36).

Horvath et al. do not teach specifically the data processing apparatus wherein data sender affixing a sequence number to each packet when sending data packets when an error occurs in data of received packet and communication error processing section requesting data sender to resend data packets based on sequence number affixed to each received packet.

However, Horst et al. teach the data processing apparatus wherein data sender affixing a sequence number to each packet when sending data packets when an error occurs in data of received packet and communication error processing section requesting data sender to resend data packets based on sequence number affixed to each received packet (see Fig. 35 and col.95, lines 47-67 and col.96, lines 1-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the data processing apparatus of Horvath et al. to include data sender affixing a sequence number to each packet when sending data packets when an error occurs in data of received packet and communication error processing section requesting data sender to resend data packets based on sequence number affixed to each received packet disclosed by Horst et al. for proper re-transmission of data packets lost due to the errors in the data processing apparatus.

7. Claims 5, 6, 8-11, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horvath et al. (US Patent Number: 5,630,056) in view of Maniwa et al. (US Patent Number: 4,860,119).

Regarding claim 5, Horvath et al. do not teach specifically the data processing apparatus further comprising a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of said reception interface sections, and wherein each of said reception interface sections receives data according to said sync signal supplied from said frequency divider.

However, Maniwa et al. teach the data processing apparatus comprising a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal (see Fig.7 and col.8, lines 19-45 wherein a sync signal generation using

frequency divider is mentioned) and sends said generated sync signal to each of said reception interface sections, and wherein each of said reception interface sections receives data according to said sync signal supplied from said frequency divider (see col.18, lines 24-63).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the data processing apparatus of Horvath et al. to include a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of said reception interface sections, and wherein each of said reception interface sections receives data according to said sync signal supplied from said frequency divider disclosed by Maniwa et al. for proper data synchronization between transmission and reception sections of the system.

Regarding claim 6, Horvath et al. teach a data processing apparatus that has a transmission interface section which transmits transmission data to a plurality of data receivers at a same timing (see col.2, lines 25-29 wherein a digital data processing device transmitting data between plural functional units is mentioned), wherein said transmission interface section generates packet data and sends individual pieces of packet data generated to said plurality of data receivers (see col.2, lines 54-59 wherein transceiver sending data to fault-detector of receivers is mentioned).

Horvath et al. do not teach specifically data processing apparatus wherein transmission interface generating packet data by dividing data to data of a data length sendable within one period of a predetermined clock signal and sending that generated data to said plurality of receivers at the same timing in synchronism with said clock signal.

However, Maniwa et al. teach a data processing apparatus wherein transmission interface generating packet data by dividing data to data of a data length sendable within one period of a predetermined clock signal and sending that generated data to said plurality of receivers at the same timing in synchronism with said clock signal (see col.18, lines 24-63).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the data processing apparatus of Horvath et al. to include transmission interface generating packet data by dividing data to data of a data length sendable within one period of a predetermined clock signal and sending that generated data to said plurality of receivers at the same timing in synchronism with said clock signal disclosed by Maniwa et al. for proper data synchronization between transmission and reception sections of the system.

Regarding claim 8, Horvath et al. do not teach specifically the data processing method wherein said data reception step and said error information output step are

executed according to a sync signal generated by dividing a frequency of a predetermined clock signal.

However, Maniwa et al. teach the data processing method wherein said data reception step and said error information output step are executed according to a sync signal generated by dividing a frequency of a predetermined clock signal (see Fig.7 and col.8, lines 19-45 wherein a sync signal generation using frequency divider is mentioned and see col.18, lines 24-63).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the data processing method of Horvath et al. to include executing data reception step and said error information output step according to a sync signal generated by dividing a frequency of a predetermined clock signal disclosed by Maniwa et al. for proper data synchronization between transmission and reception sections of the system.

Regarding claim 9, Horvath et al. further teach the data processing method comprising an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections (see col.2, lines 37-46 and lines 59-65 wherein response of transmission error among transceivers is mentioned); and a data resend requesting step of requesting said data sender to resend data in at least one of a case where an error is detected at said

error detection step and a case where error information is received at said error information reception step (see col.2, lines 32-53 wherein fault-detector signaling a fault is mentioned and wherein upon detection of an error by fault-detector, disabling of data processing by functional unit and re-transmission of respective data by processing sections are mentioned).

Regarding claim 10, Horvath et al. further teach the data processing method further comprising a data cancellation step of canceling data; and a data reception stopping step of stopping data reception, and wherein said data cancellation step and said data reception stopping step are executed in at least one of a case where an error is detected at said error detection step (see col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals is mentioned) and a case where error information is received at said error information reception step, and said data resend requesting step requests resending of data canceled at said data cancellation step (see col.2, lines 58-65 wherein upon detection of an error by fault-detector, re-transmission of serial data by transceiver to fault-detector is mentioned).

Regarding claim 11, Horvath et al. teach data cancellation step of the data processing method (see col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals is mentioned) and do not teach specifically the said data cancellation step is executed according to said sync signal.

However, Maniwa et al. teach the data processing method wherein sync signal is used for outputting data (see col.18, lines 24-63).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the data processing method of Horvath et al. to include executing data cancellation step according to said sync signal disclosed by Maniwa et al. for proper data synchronization between transmission and reception sections of the system.

Regarding claim 13, Horvath et al. teach the computer readable medium according to claim 12, executing said data reception step and said error information output step as applied to claim 12.

Horvath et al. do not teach specifically said data reception step and said error information output step are executed according to a sync signal generated by dividing a frequency of a predetermined clock signal.

However, Maniwa et al. teach execution of outputting data according to a sync signal generated by dividing a frequency of a predetermined clock signal (see Fig.7 and col.8, lines 19-45 wherein a sync signal generation using frequency divider is mentioned and col.18, lines 24-63 for outputting data as per sync signal is mentioned).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the execution of computer readable medium according to claim 12, to include executing said data reception step and said error information output step according to a sync signal generated by dividing a frequency of a predetermined clock signal disclosed by Maniwa et al. for proper data synchronization between transmission and reception sections of the system.

Regarding claim 14, Horvath et al. further teach the computer readable medium according to claim 13, executing an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections (see col.2, lines 37-46 and lines 59-65 wherein response of transmission error among transceivers is mentioned); and a data resend requesting step of requesting said data sender to resend data in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step (see col.2, lines 32-53 wherein fault-detector signaling a fault is mentioned and wherein upon detection of an error by fault-detector, disabling of data processing by functional unit and re-transmission of respective data by processing sections are mentioned).

Regarding claim 15, Horvath et al. further teach the computer readable medium according to claim 14, executing a data cancellation step of canceling data; and a data reception stopping step of stopping data reception, and wherein said data

cancellation step and said data reception stopping step are executed in at least one of a case where an error is detected at said error detection step (see col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals is mentioned) and a case where error information is received at said error information reception step, and said data resend requesting step requests resending of data canceled at said data cancellation step (see col.2, lines 58-65 wherein upon detection of an error by fault-detector, re-transmission of serial data by transceiver to fault-detector is mentioned).

Regarding claim 16, Horvath et al. teach the computer readable medium according to claim 15, executing data cancellation step (see col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals is mentioned) and do not teach specifically the said data cancellation step is executed according to said sync signal.

However, Maniwa et al. teach the execution wherein sync signal is used for outputting data (see col.18, lines 24-63).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the execution of computer readable medium according to claim 15 of Horvath et al. to include executing data cancellation step according to said sync signal

disclosed by Maniwa et al. for proper data synchronization between transmission and reception sections of the system.

Response to Arguments

8. Applicant's arguments filed on March 11th, 2008 have been fully considered but they are not persuasive.

9. In page 7, Applicants mention that Horvath fails to teach an apparatus with reception interface sections that receive the same data from a same data sender in parallel. However, Horvath et al. teach an apparatus with reception interface sections that receive the same data from a same data sender in parallel (see col.3, line 60 to col.4, line 2 wherein functional units i.e. processor/memory elements 10, 12 **partnered with one another to respond concurrently and identically to information input from bus** 20 to generate further information for output to bus 20 is mentioned, likewise peripheral device controllers 14, 16 partnered with one another to process and communicate like information between the functional units and peripheral devices is mentioned. And also see col.2, lines 25-32 wherein a digital data processing device with plurality of functional units processing data in parallel is mentioned and col.2, lines 54-59 wherein transceivers, which include both transmitters and receivers, routing data is mentioned).

10. In page 8, Applicants mention that Horvath does not teach reception interface sections at all. However, Horvath et al. teach clearly the processing sections include transceivers (see col.2, lines 54-56), which include both transmitting section and receiving sections.

11. In page 9, Applicants mention that Horvath specifically failing to teach an apparatus that, "upon occurrence of an error in said received data, stops receiving said data, sends a communication error signal to other reception interface sections to stop data reception from said data sender, and requests said data sender to resend data."

However, Horvath et al. teach the above limitation (see col.2, lines 32-36 wherein fault-detector signaling a fault is mentioned and col.2, lines 47-53 wherein upon detection of error, functional unit disabling the processing sections further from applying signals and responding to the error by reapplying the data is mentioned. And also Fig.1 and col.3, line 55 to col.4, line 2 wherein functional units i.e. processor/memory elements 10, 12 **partnered with one another to respond concurrently and identically** to information input from bus 20 **to generate further information for output to bus 20** is mentioned, likewise peripheral device controllers 14, 16 partnered with one another to process and communicate like information between the functional units and peripheral devices is mentioned). The explanation in above sections i.e. 9, 10 and 11 apply to Applicant's remarks w.r.t. claims 1-3, 7, and 12 and the rejection of these claims is already explained above under Claims Rejections.

12. Regarding claim 4 in page 9, applicants mention that both Horvath and Horst fail to teach the data processing apparatus as per the claim. However, Horvath et al. and Horst et al. together teach the data processing apparatus as per the claim 4 as explained above under Claim Rejections for this claim. Applicants mention that there is no teaching or suggestion in the passage, or anywhere else in the disclosure of Horst,

that an apparatus, "upon occurrence of an error in said received data, stops receiving said data, sends a communication error signal to other reception interface sections to stop data reception from said data sender, and requests said data sender to resend data". However, Horvath et al. teach this as explained in section 11 above.

13. Regarding claims 5, 6, 8-11 and 13-16 in page 10, Applicants mention that Maniwa and Horvath are not analogous art and submit that one of ordinarily skill in the art of parallel data processing, the field of the invention, would not think it obvious to look to the field of image formation and printing to combine teachings to augment those teachings found in field of parallel data processing. However, Maniwa's image formation & printing involves data storing and processing techniques which can be applied to Horvath's parallel data processing also for enhancing or improving performance of the system. Applicants further mention that there is no teaching or suggestion in Maniwa of an apparatus that has a plurality of reception interface sections
"which receive same data from a same data sender" in parallel, wherein, "upon occurrence of an error in said received data, stops receiving said data, sends a communication error signal to other reception interface sections to stop data reception from said data sender, and requests said data sender to resend data". However, Horvath et al. teach this as explained in section 11 above.

14. In page 11, Applicants mention that there is no teaching or suggestion in these passages, or anywhere else in the disclosure of Maniwa, of an apparatus that, upon

receiving an error is received data, a communication signal is sent to other reception interface sections to stop data reception. However, Horvath et al. teach this as explained in section 11 above.

15. In page 12, Applicants mention for claim 6 that there is no teaching or suggestion by Horvath in the passage of that the transmission data is transmitted to the plurality of data receivers at a same timing. However, Horvath et al. teach this (see col.2, lines 25-29 wherein a digital data processing device transmitting data between plural functional units is mentioned & also see col.2, lines 54-59 wherein transceiver sending data to fault-detector of receivers is mentioned.) Also see the explanation in section 11 above.

16. In page 13, Applicants mention that for claim 6, Maniwa fails to teach a plurality of receivers, or that data is sent to a plurality of receivers in sync with the clock signal, and at a same timing. However, **Horvath et al. and Maniwa et al.** together teach "a data processing apparatus that has a transmission interface section which transmits transmission data to a plurality of data receivers at a same timing, wherein said transmission interface section generates packet data by dividing said transmission data to data of a data length sendable within one period of a predetermined clock signal and sends individual pieces of packet data generated to said plurality of data receivers at the same timing in synchronism with said clock signal" as explained under the Claim Rejections above for this claim. Also, see the further explanation in section 11 above for transmission of data to a plurality of data receivers at the same timing.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

18. Any response to this office action should be faxed to (571) 273-8300 or mailed To:

Commissioner for Patents,
P.O. Box 1450
Alexandria, VA 22313-1450
Hand-delivered responses should be brought to
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SRINIVASA R. REDDIVALAM whose telephone number is (571)270-3524. The examiner can normally be reached on Mon-Fri 9:30 AM - 7 PM (1st Friday OFF).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on 571-272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

S Reddivalam
05/25/2008

/Chirag G Shah/
Supervisory Patent Examiner, Art Unit 2619